FIG. 1

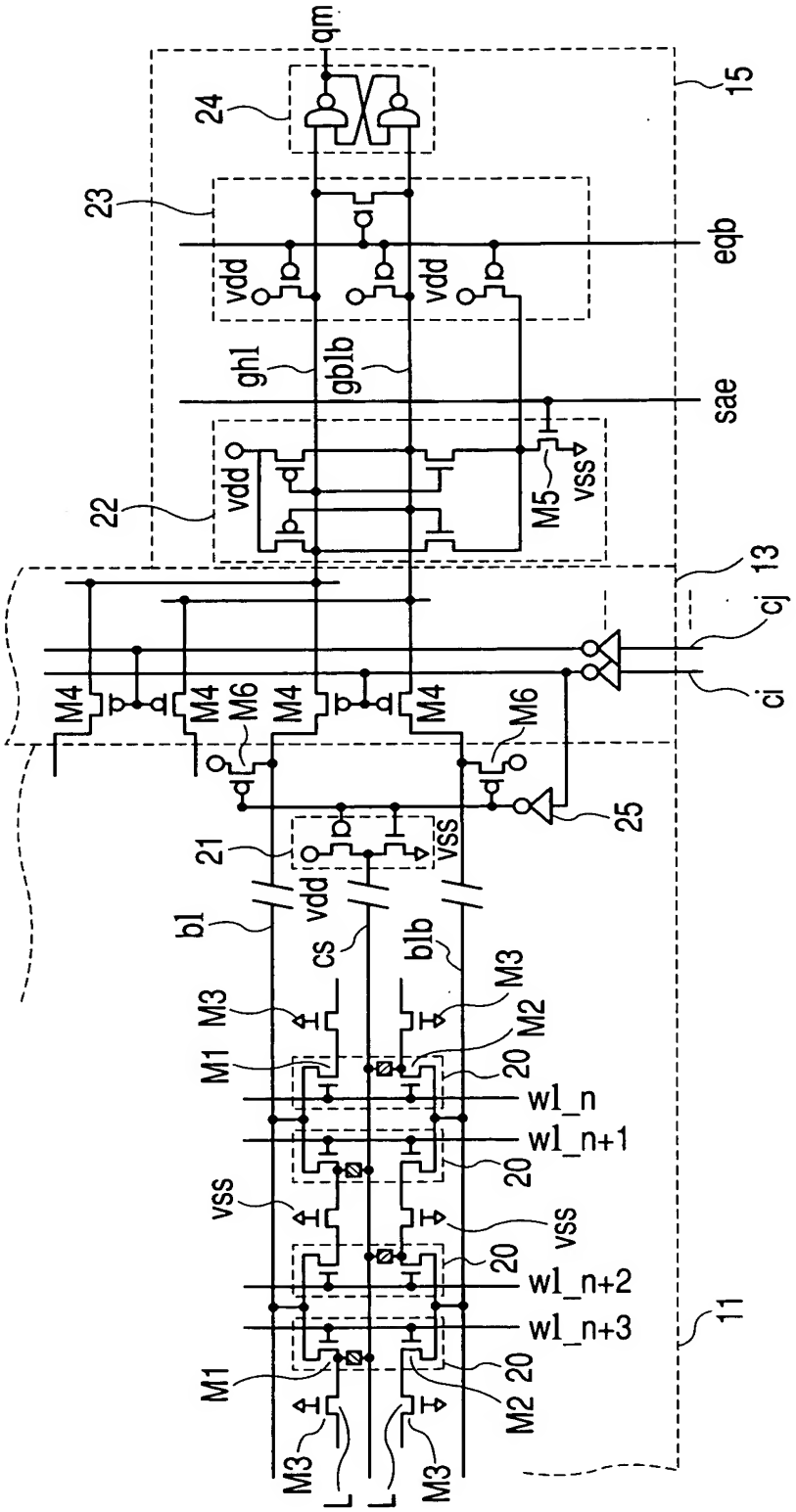

qm
24
15
23
eqb
vdd
vdd
ghl
gblb
sae
22
vdd
M5
vss
13
cj
ci
M4
M4
M6
M4
M4
M6
25
21
vss
vdd
bl
cs
blb
M3
M3
M2
M1
20
wl_n
wl_n+1
vss
vss
20
wl_n+2
wl_n+3
11
M1
20
M2
M3
M3
L
L

FIG. 2

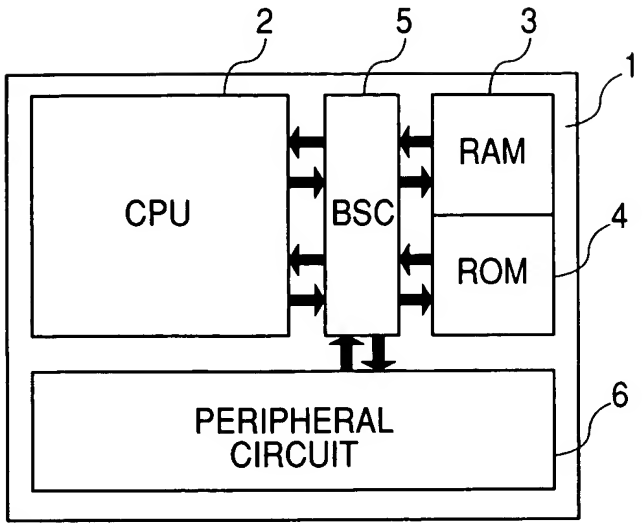

2
5
3
1
CPU
BSC
RAM
ROM
4
PERIPHERAL CIRCUIT
6

FIG. 3

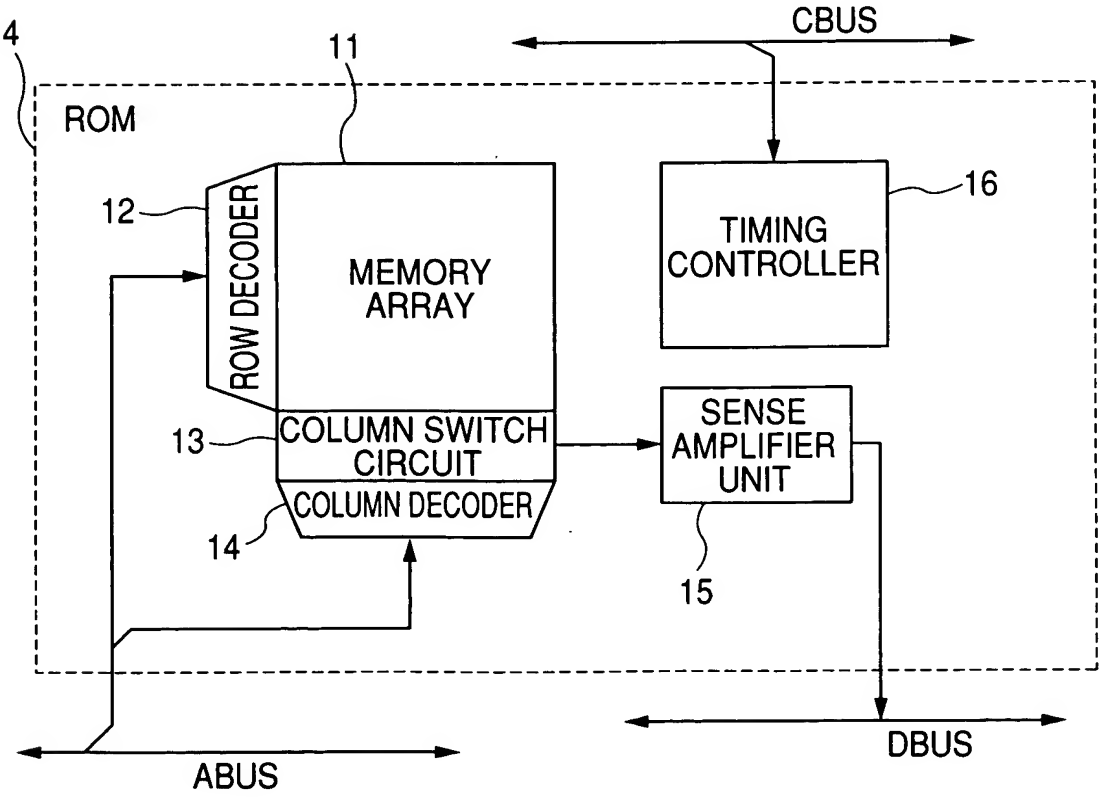

4
11
CBUS
ROM
12
ROW DECODER
MEMORY ARRAY
TIMING CONTROLLER
16
13
COLUMN SWITCH CIRCUIT
SENSE AMPLIFIER UNIT
COLUMN DECODER
14
15
ABUS
DBUS

FIG. 4

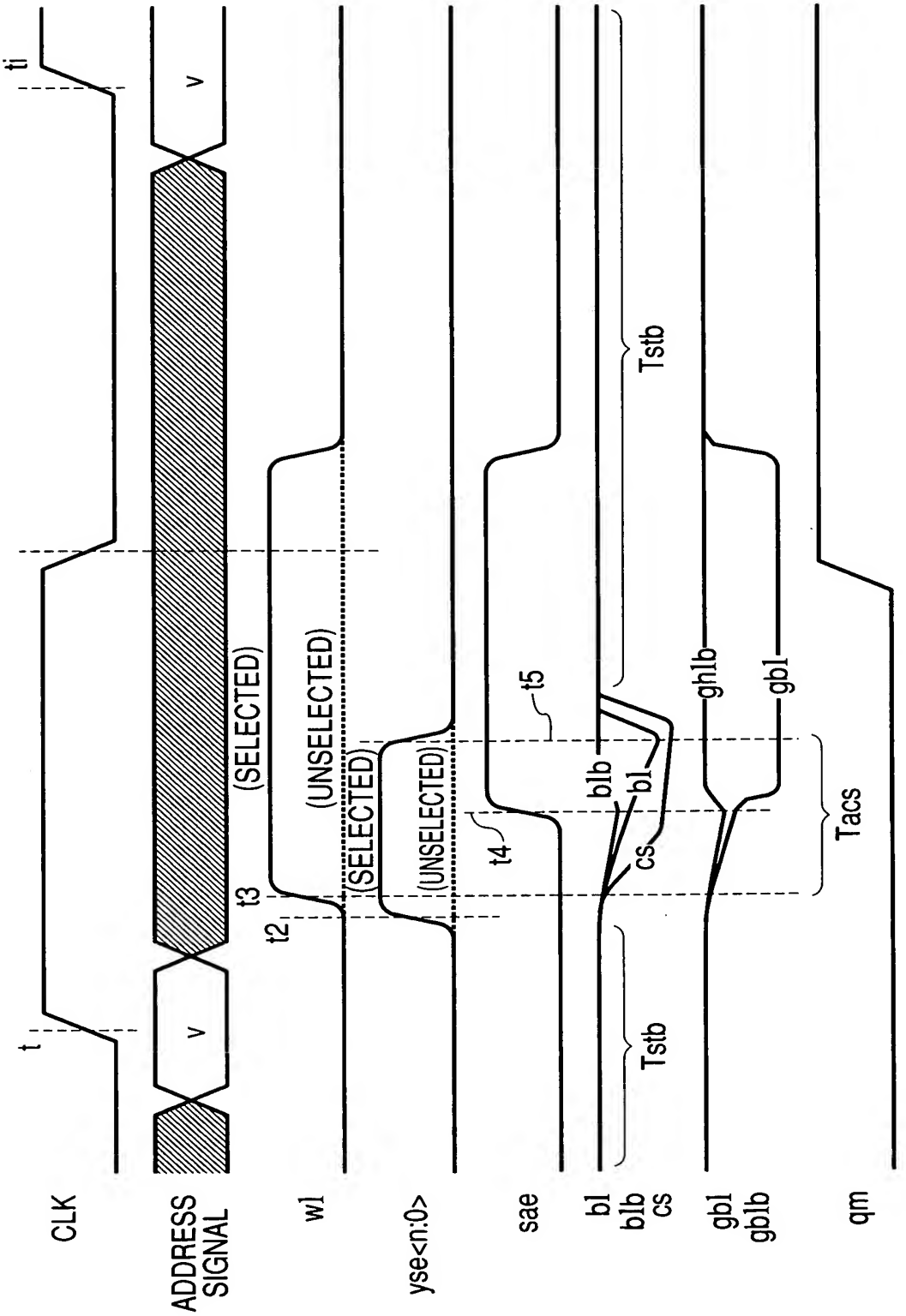

CLK
ADDRESS SIGNAL
wl
yse<n:0>
sae
bl
blb
cs
gbl
gblb
qm
ti
t
v
v
(SELECTED)
(UNSELECTED)
(SELECTED)
(UNSELECTED)
t2
t3
t4
t5
Tstb
Tstb
Tacs
blb
bl
cs
gblb
gbl

FIG. 5

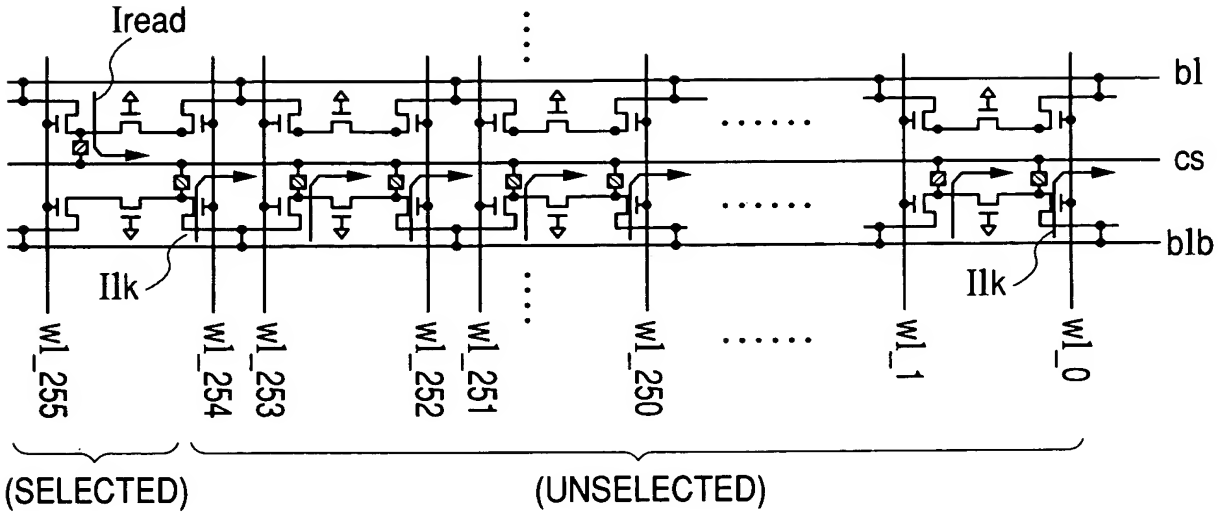

Iread
bl
cs
blb
Ilk
Ilk
wl_255
wl_254
wl_253
wl_252
wl_251
wl_250
wl_1
wl_0
(SELECTED)
(UNSELECTED)

FIG. 6

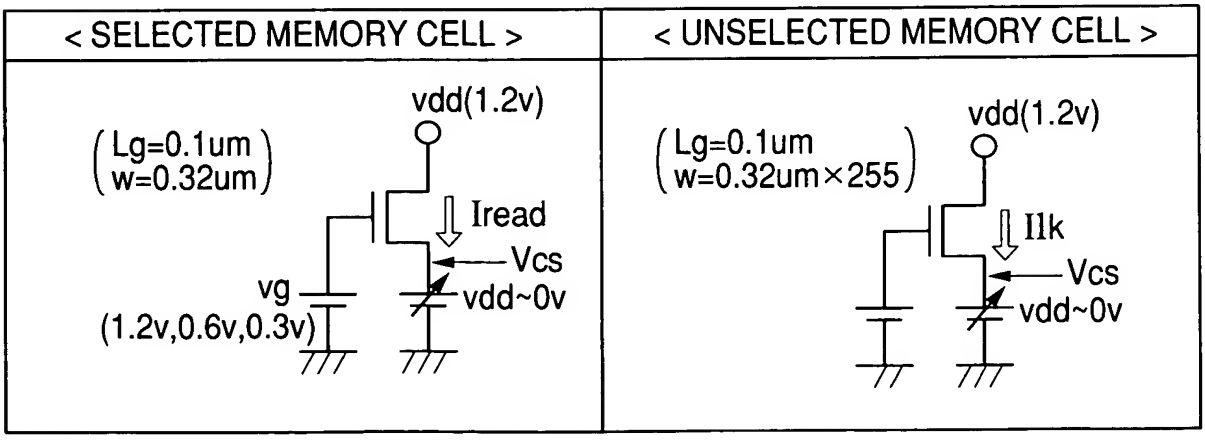

< SELECTED MEMORY CELL >
< UNSELECTED MEMORY CELL >
vdd(1.2v)
(Lg=0.1um
w=0.32um)
Iread
Vcs
vg
(1.2v,0.6v,0.3v)
vdd~0v
vdd(1.2v)
(Lg=0.1um
w=0.32um×255)
Ilk
Vcs
vdd~0v

FIG. 7

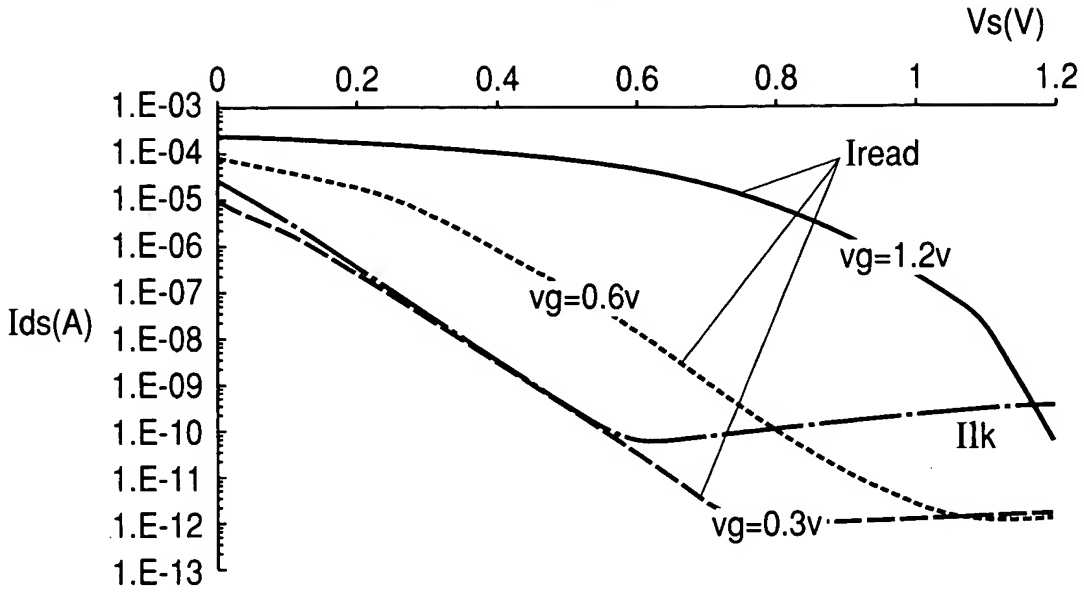

Vs(V)
0
0.2
0.4
0.6
0.8
1
1.2
1.E-03
1.E-04
1.E-05
1.E-06
1.E-07
1.E-08
1.E-09
1.E-10
1.E-11
1.E-12
1.E-13
Ids(A)
Iread
vg=1.2v
vg=0.6v
Ilk
vg=0.3v

FIG. 8

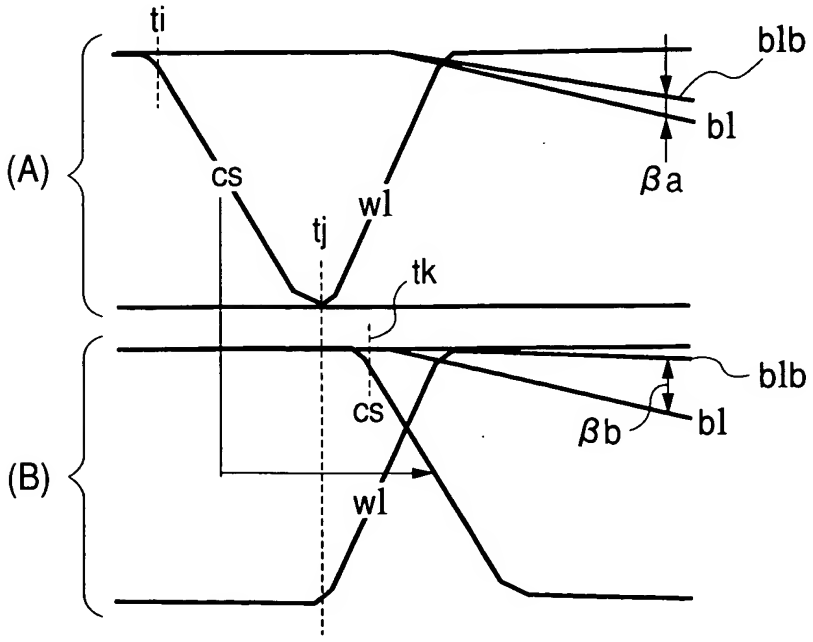

ti
blb
bl
(A)
cs
βa
wl
tj
tk
blb
cs
βb
bl
(B)
wl

FIG. 9

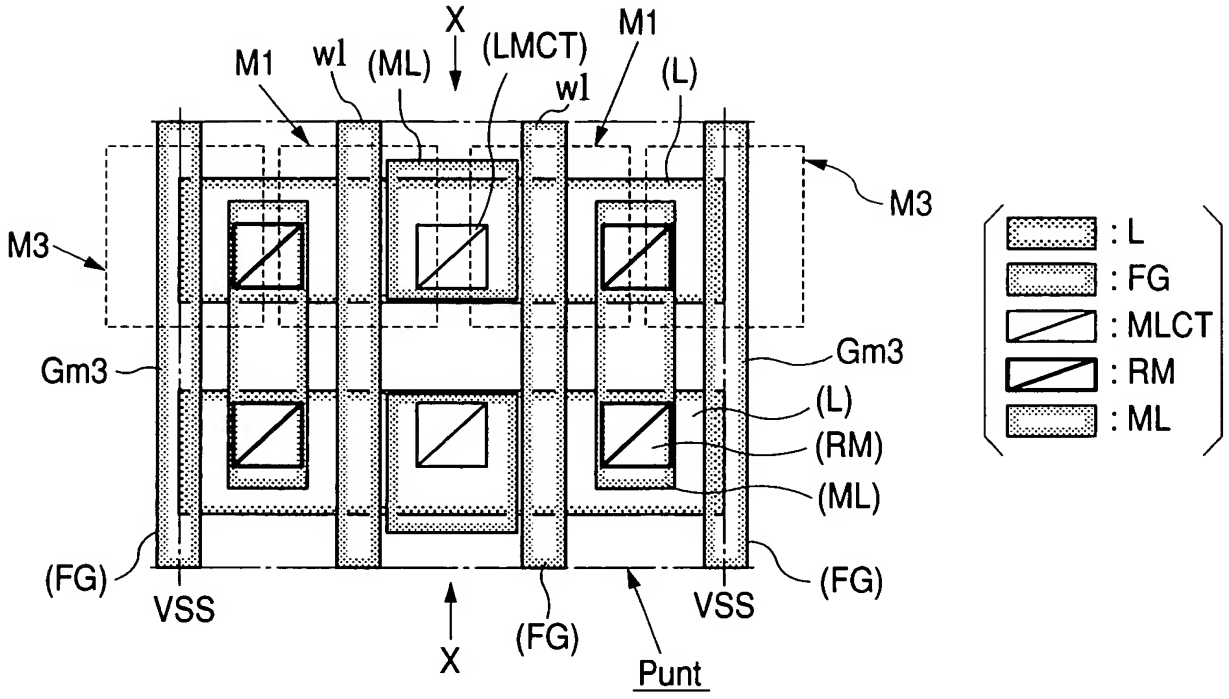

X
M1
wl
(ML)
(LMCT)
wl
M1
(L)
M3
M3
Gm3
Gm3
(L)
(RM)
(ML)
(FG)
VSS
X
(FG)
VSS
(FG)
Punt
: L
: FG
: MLCT
: RM
: ML

FIG. 10

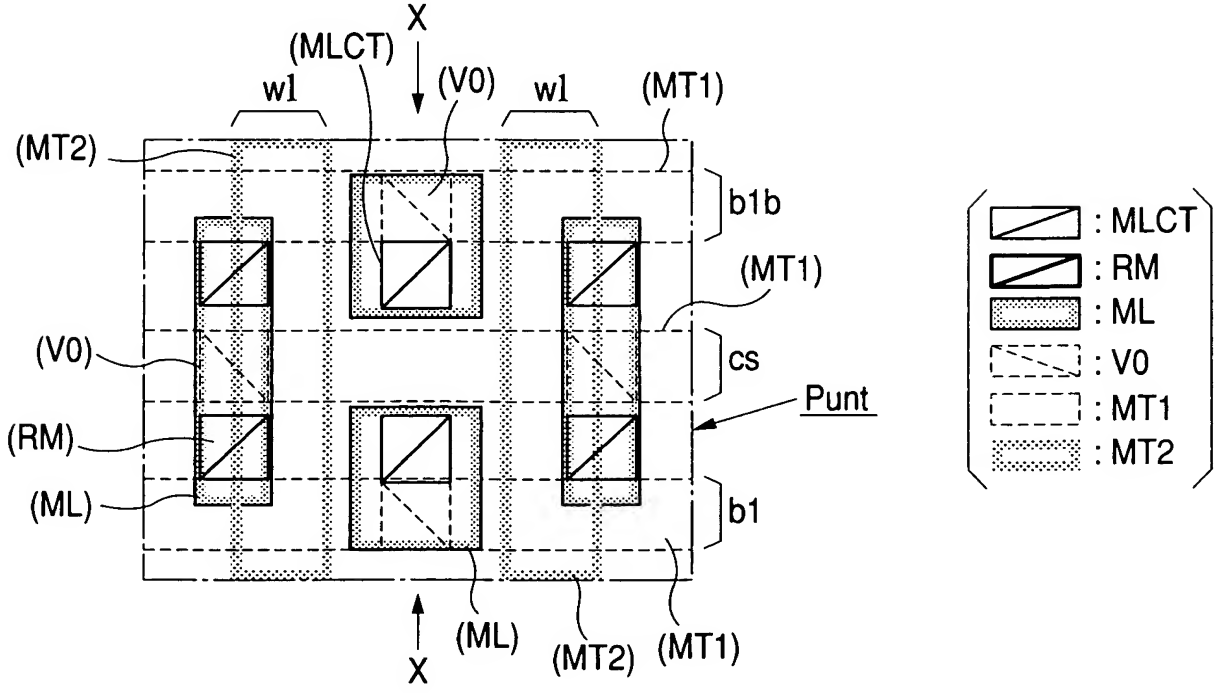

X
(MLCT)
wl
(V0)
wl
(MT1)
(MT2)
b1b
(MT1)
(V0)
cs
Punt
(RM)
(ML)
b1
X
(ML)
(MT2)
(MT1)
: MLCT
: RM
: ML
: V0
: MT1
: MT2

FIG. 11

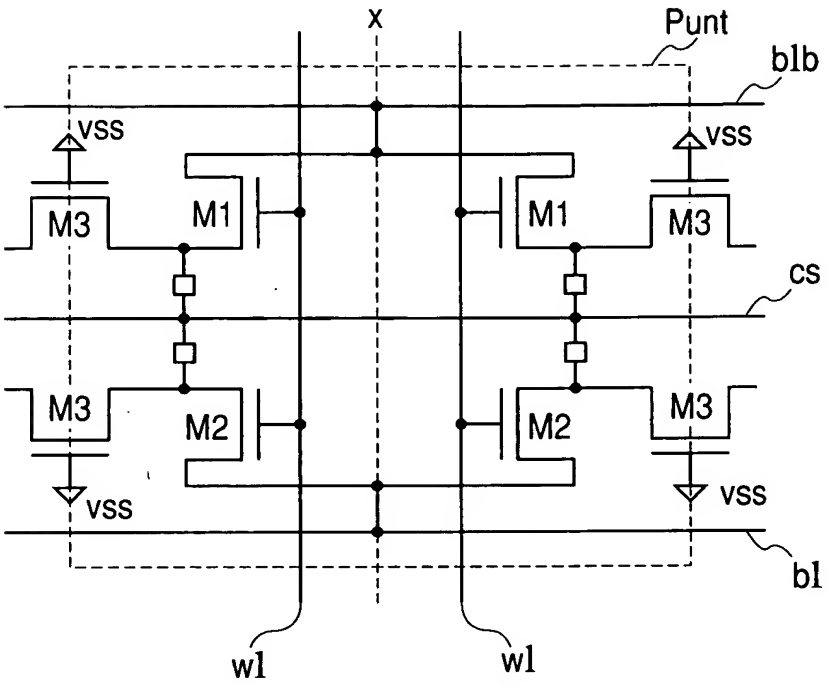

x
Punt
blb
vss
vss
M3
M1
M1
M3
cs
M3
M2
M2
M3
vss
vss
bl
wl
wl

FIG. 12

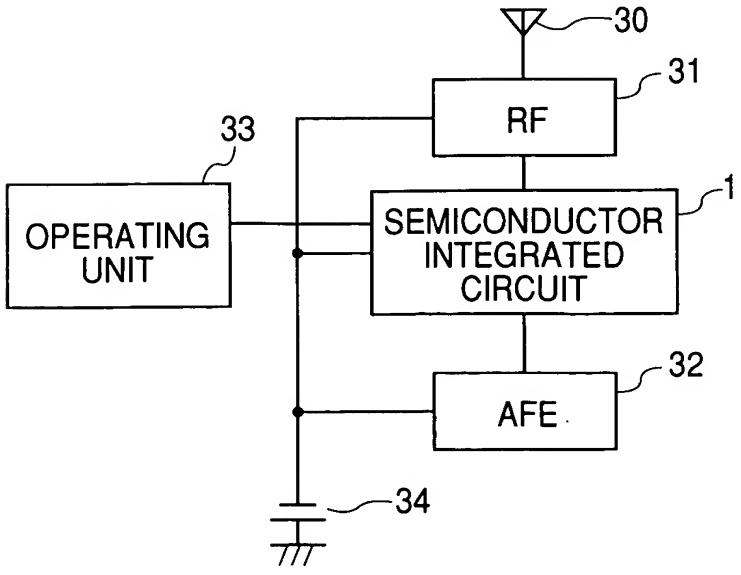
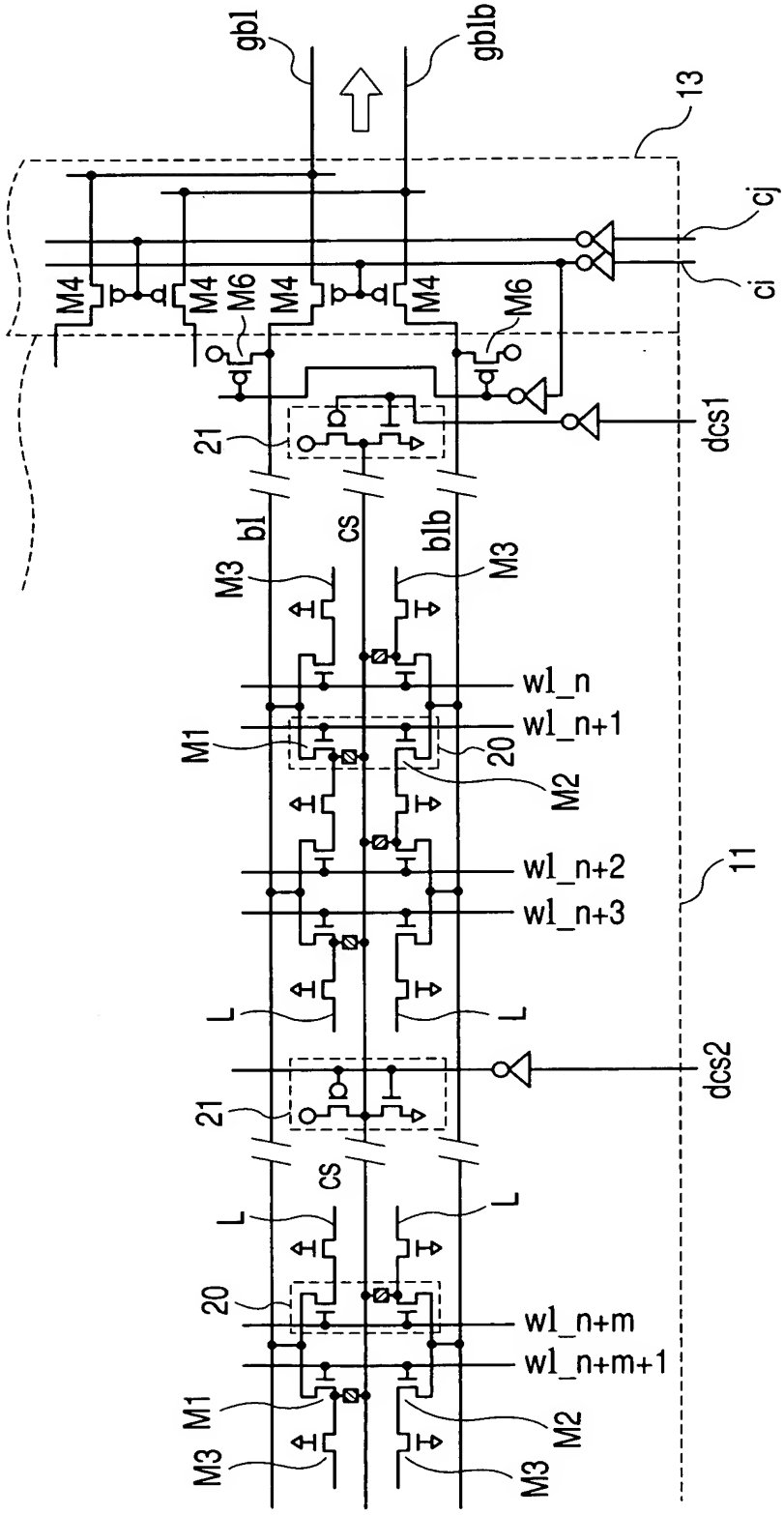

30
31
RF
33
OPERATING UNIT
SEMICONDUCTOR INTEGRATED CIRCUIT
1
32
AFE
34

FIG. 13


gbl
gblb
13
cj
ci
M4
M6
dcs1
21
bl
cs
blb
M3
wl_n
wl_n+1
M1
20
M2
wl_n+2
wl_n+3
11
L
dcs2
wl_n+m
wl_n+m+1